NATIONAL BUREAU OF STANDARDS REPORT

2794

SEAC MAINTENANCE MANUAL

THE OUTSCRIBER

by

Russell A. Kirsch

U. S. DEPARTMENT OF COMMERCE
NATIONAL BUREAU OF STANDARDS

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NBS

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I. INTRODUCTION

One of the more serious problems in the design of automatic digital computers is that of getting the calculated results out of the machine rapidly enough to avoid delaying the further progress of the calculations. In many of the problems to which a general-purpose computer is applied the amount of output data is relatively great -- so great that serious inefficiency would result from forcing the computer to wait for these data to be typed on existing printing devices. This difficulty has been solved in the SEAC* by providing magnetic recording devices as output units. These devices are able to receive information from the machine at rates up to 100 times as fast as an electric typewriter can be operated. Thus, better efficiency is achieved in recording the output data; transcription can be made later from the magnetic recording device to a printing device without tying up the main computer.

In the SEAC the output magnetic recording device used is a magnetic wire unit in which the magnetic wire is held in a cartridge which can be conveniently and quickly removed from the recording unit. Then, when the recorded wire is to be transcribed to produce the printed copy, this magnetic wire cartridge is inserted in a special unit called an "Outscriber" which serves to read the magnetically recorded data and put it in a form acceptable to the printer. In the SEAC installation the Outscriber prepares a punched paper tape which then can be used to operate an automatic typewriter such as a Flexowriter or a Teletype printer.

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* National Bureau of Standards Eastern Automatic Computer.

Punched paper tape is used as an intermediary (rather than connecting the Outscriber directly to the printer) primarily to provide a "time buffer" between the magnetic wire and the printer. For the available printers certain operations such as Tabulation and Carriage Return require significantly greater time than the typing of a single character. Thus if the magnetic wire were to be read at rates comparable to the typing rate of the printer, when a Carriage Return should occur, it would be necessary either to force the magnetic wire to pause or to store considerable extra information to smooth out the interruption in the printer operation. This would lead to mechanical difficulties in the magnetic wire drive which are obviated by the use of the punched paper tape intermediary.

A second purpose for the punched paper tape is in anticipation of the future operation of the Outscriber with tape punches operating six to ten times the speed of automatic typewriters. With this operation, a single Outscriber could keep several typewriters busy. This report describes the Outscriber that was built for the SEAC installation, that is, the device that produces punched paper tape from the information on the magnetic wire.

II. GENERAL DESCRIPTION OF THE OUTSCRIBER

The main components of the Outscriber are shown in the block diagram of Figure 1, in which the flow of information in the machine is indicated by the interconnecting lines. The following paragraphs provide a general explanation of the function of the major parts of the machine, indicated as blocks in the figure.

Originally, the desired information is recorded magnetically on wire in SEAC. In the Outscriber, this wire is driven past a reading head in the Wire Drive. The output of the reading head coil is a very small voltage, which is amplified in the Amplifier. The amplifier is necessary because the voltage signal from the reading head is too small to be used by the rest of the circuitry. In the main part of the Outscriber, the circuitry used is of a type similar to that used in SEAC. In order to drive this circuitry, it is necessary to produce short sharp pulses, which is done in what is called the Channel Pulse Generator. These pulses, however, may occur at widely varying times. If the wire should speed up or slow down, there will be a change in the time between successive pulses. However, it is necessary that pulses should occur only when the clock pulses occur, i.e., the output of the channel pulse

generator must be synchronized with the one-megacycle clock. This is accomplished in the Synchronizer. The output of this circuit is a short train of pulses, which occurs during the channel pulses, with each pulse of the train coinciding with a clock pulse.

For each binary digit on the wire, there occur exactly two channel pulses. In order to group the channel pulses so as to correspond to binary digits, it becomes necessary to divide them into groups of two. This is done in the Binary Counter.

At this point in the discussion, it may be assumed that the machine has identified the binary digits as either ones or zeros. The final problem to be solved is the grouping of these binary digits in such a fashion that a punch may prepare a paper tape with the desired information. To do this, the information is first fed serially into the Shift Register, i.e., the binary digits are fed in one at a time. When four such digits have entered the shift register, the information is transferred in parallel into a row of Buffer Flip-Flops, i.e., all four binary digits are read out simultaneously. The buffer flip-flops drive a row of Relays which in turn operate the Punch. As a result, four binary digits (or one hexadecimal character as such a group is called) are punched in each cycle of the punch. The punched tape that is produced has four rows of information on it.

Because of the way in which information is grouped on the wire, it is possible to perform an error check on the operation of the Outscriber electronic circuitry. Information recorded on the wire is grouped into "words", each of which consists of 52 binary digits (13 hexadecimal characters). Recordings are made with groups of integral numbers of these words and with gaps between these groups. When a gap occurs, the shift register and the binary counter are sensed. Since the number of binary digits that occur between gaps is a multiple of four, a multiple of four binary digits should have been read into the shift register. But every time four binary digits get into the shift register they are read out into the buffer flip-flops. Therefore, the shift register should be empty of binary digits when the gap arrives on the wire. It is the function of the Error Checking Circuit to check for this condition. In case an error is detected, the wire is halted and an indication is given to the operator that the error has occurred.

III. CONSTRUCTION

The Outscriber is built in two units, as indicated in Figure 2. The smaller of the two racks contains the following equipment:

1. A Flexowriter punch.
2. A tape feed mechanism to supply paper tape for the punch.
3. A power bleeder which provides filtered computer voltages from the 220-volt d-c line.
4. A blower for cooling the resistors in the power bleeder.

The main rack contains the following equipment:

1. An amplifier to amplify the output of the reading head.
2. An oscilloscope which is used for monitoring the output pulses from the amplifier.
3. A chassis on which are located the package circuitry which performs all logical functions, the special wave-shaping circuits, and the relays for driving the punch.
4. An operator's control panel on which all switching functions are performed.
5. An a-c power strip.
6. A Pierce wire drive with four wire speeds.
7. A regulated 235-volt d-c supply which furnishes plate voltage for the packages, the amplifier, and the special wave-shaping circuits.
8. An unregulated power supply which furnishes 110 volts d-c for the control voltages on the punch and 300 volts d-c for the control voltages on the wire drive.
9. A blower for cooling the packages.

All interconnecting cables are shown in Figure 2. In the Outscriber, these cables are either labeled or color-coded to facilitate the making of proper connections.

On the main chassis, wiring is of two types -- open and packaged. Connections within individual packages are shown in Drawing No. G-3C. Important points in the wiring are brought out to test points on a terminal strip. Some of these test points require jumpers on the terminal strip. The test points are indicated by circled numerals on Drawing No. 204C. The corresponding numbers with the designation of the signal leads they represent are shown on the terminal strip.

IV. DETAILED DESCRIPTION OF THE OUTSCRIBER

A. Special Circuits

The information that is to be punched is originally in the form of spots of magnetization along an 1,800-foot length of wire which is driven at the rate of 1.2 inches per second past a reading head in the wire drive. When the wire is driven at this speed, the output of the reading head is approximately 200 microvolts. There are about 33 pulses per inch on the wire, so that when it is run at 1.2 inches per second, there are 40 pulses read each second or, equivalently, 10 hexadecimal characters.

The low output of the reading head must be amplified to drive pulse-shaping circuits. The amplification for this purpose is obtained from a double-channel four-stage amplifier with a high degree of degeneration between opposite halves of each stage. This results in two outputs from the last stage that are the inverse of each other. The schematic of this amplifier is given in Figure 3.

The purpose of some of the pulse-shaping circuitry following the amplifier is to provide sharp uniform pulses that can be used by subsequent high-frequency computer-type circuitry to identify wire pulses as zeros and ones. In order to produce these sharp information pulses, the amplifier outputs are each d-c coupled into a Schmitt circuit. Under no-signal conditions the first tube of the Schmitt pair has its grid at -26 volts with respect to its cathode so that the tube is cut off. The following tube is heavily conducting, and its output voltage taken from the plate is correspondingly low.

Consider now that a "one" pulse is read by the head and appears (in essentially the same form) at the amplifier output to one of the Schmitt pairs. In Drawing No. 204C the two Schmitt pairs constitute tubes V2.2 and V2.1 and their associated circuits. The voltage levels of the incoming signal are indicated in Figure 4b. When this signal reaches triggering level (123 volts), the states of the two triodes in V2.2 undergo a rapid reversal, the first tube conducting and the second being cut off. The plate voltage of the second tube has a rise time of 5 or 6 microseconds. It is necessary that this rise be sharp in order to drive the pulse stage that follows.

The state of the pair of tubes remains fixed thereafter until the signal level falls to 116 volts. Note that the Schmitt circuits are so designed that they should trigger into their unstable state at a higher voltage than that at which they return to equilibrium. This "hysteresis", or difference between the triggering levels, should be about 7 volts, a value which is larger than that of most spurious pulses that may come out of the amplifier.

The same operation as above occurs in V2.1 during the second half of the cycle corresponding to a single digit on the wire. Thus the Schmitt circuits produce two square waves for each wire pulse. The first square wave appears at the output of that channel which first goes positive. The second square wave begins when the other channel goes correspondingly positive. It can be seen, then, that a "one" pulse on the wire will cause channel a to produce a square wave first and then channel b to produce a similar one, whereas a "zero" pulse on the wire will cause these roles to be reversed.

Each of these square waves is differentiated by a .01-μfd capacitor and 62K resistor combination, the output corresponding to the pulse rise being considerably larger than that occurring during the time the Schmitts trigger back to their first state.

The pulses from each of the differentiating circuits are used to drive pulse amplifier stages, each stage consisting of a 6AN5 tube and a stepdown transformer. The output pulse from this transformer is the information (or channel) pulse, Ia or Ib, mentioned previously. It is of a voltage and at an impedance level appropriate for driving the standard computer circuitry that follows. It is necessary that the information pulses be of at least three microseconds duration in order properly to drive the logical circuitry that will be described later. This is accomplished by using a 170:24 stepdown transformer as the output from the channel stage. The voltage waveform of this pulse and those of the other points in the pulse-shaping circuits just discussed can be seen in Figure 4.

Before considering the computer-type circuitry that performs logical operations on the information pulses Ia and Ib, a circuit whose function is to produce an output voltage that rises when the machine is ready to sense for an error will be discussed. This circuit is the Gap Senser. Since pulses are usually recorded in groups of eight words with small spacing between pulses but relatively long spaces between eight-word groups, it becomes convenient to check the machine for errors every time one of these "gaps" occurs.

The circuitry for producing this voltage consists of V 2.5, a 12AU7 type tube, and its associated components shown in Drawing No. 204C. The waveforms mentioned can be seen in Figure 5. A two-input diode OR-gate allows the square-wave outputs of the Schmitt tubes to appear on the left hand plate of the 0.25-μfd coupling capacitor. Between this capacitor and the grid of the first gap senser tube (V2.5a) is a coupling circuit the purpose of which is to allow the 0.25-μfd capacitor to charge and discharge at the same rate.

The output of the coupling circuit drives a cathode follower (V2.5a) whose output, upon swinging negative, charges a 0.2-μfd capacitor negatively through the low impedance path consisting of a 1.0-μfd capacitor and a diode conducting in its forward direction. So long as pulses continue to appear at the output of V2.5a, the 0.2-μfd capacitor retains its negative charge. When the output pulses cease, however, this capacitor slowly begins to discharge to +4 volts through a 200K resistor. The voltage on this capacitor is used to drive a cathode follower (V2.5b) whose output is clipped at -8 volts.

The critical factor in the operation of this circuit is the behavior in response to the first pulse after a gap. It is necessary that this pulse cause the 0.2-μfd capacitor to become charged sufficiently negative that the output of V2.5b drops to -8 volts and remains there until the next gap.

B. SEAC-Type Circuits

As previously mentioned, the circuitry of the Outscriber is of two types. The first type, most of which has thus far been described, is peculiar to the Outscriber. The second type is the same as that used to perform logical functions in SEAC. This part of the circuitry is shown in Drawing No. 204C.

The two information pulses Ia and Ib occur at times determined by the mechanical peculiarities of the wire drive. It is necessary that these pulses be synchronized with the four-phase clock of the Outscriber before they may be used in the logical circuitry. To do this, the synchronizer (Drawing No. 204C) gates the two information pulses with a narrow clock pulse. A special regeneration circuit allows the T1 stage to produce 3/4-microsecond pulses only while Ia or Ib are above gating level. Ia and Ib last long enough to produce three such pulses. T1 drives a driver stage T2 which produces a standard 1/2-microsecond pulse for each incoming pulse from T1. Figure 6 shows this timing graphically.

It will be recalled that all information as to the presence of binary "ones" or "zeros" is obtained from the two pulses Ia and Ib. Since each wire pulse has both a corresponding Ia and Ib, a "one" can be distinguished from a "zero" by the fact that for a "one" Ia occurs before Ib, whereas the reverse is true for a "zero". The first function of the logical circuitry, then, is to count these information pulses (Ia and Ib) and to provide a signal that can be used to group them into pairs that correspond to wire pulses. This is done in the binary counter.

The operation of the circuitry can be seen by referring to Figure 6 and the schematic of the binary counter in Drawing No. 204C. The first pulse from T2 causes the top AND-gate, which drives the B stage, to turn the B stage on. Recirculation of this pulse is maintained by means of the bottom AND-gate until T2 goes off. Then recirculation is maintained by means of the middle AND-gate. The result is that the B stage produces a pulse train that remains on.

Sometime later, however, in the order of four milliseconds, Ib occurs and by the same process as just described causes three more T2 pulses to be produced. The first of these T2 pulses turns off the B stage which remains off until the next binary digit is read from the wire. At that time a new Ia and Ib will occur and the operation will be repeated.

The significant function of this circuitry is that it takes information pulses which occur at entirely asynchronous times and enables these pulses to drive a stage that is turned on with every second pulse. When the output of this "binary counter" B goes off, a new binary digit is known to have occurred.

Before investigating the way in which the "ones" and "zeros" are fed into the shift register, two more signals, used in the shift register, must be considered. The shift pulse S is generated when B is turned off. It is a single pulse occurring during CP3 time, simultaneously with an identical pulse -H (for "hold"). The timing of these pulses is shown in Figures 6 and 7. Their use will become apparent in the discussion of the shift register, which consists of stage Rm and flip-flops R1 through R6.

Let us consider what happens in stage R1 of the shift register, and in particular, the operation of the AND-gate whose inputs are Ib and S. If the second of the information pulses (the one that produced S), is an Ib, then this gate will turn R1 on; that is, it will put a binary "one" in R1. If this second pulse is an Ia, i.e., if Ib occurred before Ia, then R1 will not be turned on and a "zero" is read into the stage.

At the same time that a "one" or a "zero" is read into R1, two things occur. S going on allows the information that was previously in R1 to feed into R2. Also,-H going on inhibits the regeneration of the old information in the R1 flip-flop. Hence, a new binary digit is read into R1 and the information that was previously in each of the stages of the register is transferred to the subsequent stage.

It will be noted that provision is made for either four or six-channel operation. For use with ordinary hexadecimal notation as is presently used in SEAC, four-channel operation is desired. If, however, it is desired to enlarge the notation to include both decimal numbers and alphabetical characters, then six-channel operation becomes necessary. This flexibility is obtained through the use of a channel switch that shunts stages R5 and R6 of the register in four-channel operation.

For the sake of simplicity, further discussion will assume that switches are set for four-channel operation unless otherwise stated. In four-channel operation, the shift register consists of five stages. The extra stage is used for a marker pulse. Assume for the time being that before the first wire pulse arrives, there is a "one" which acts as a marker pulse in R1. When the fourth wire pulse arrives, this marker will be shifted into the Rm stage. This stage is not a flip-flop, as are stages R1-R6, because it is at no time necessary to retain information in Rm for more than one microsecond.

When the marker arrives in Rm, the stage output opens the gates to the buffer flip-flops F1 through Fm. Whatever information is in stages R1 through R4 and Rm will be fed in parallel into F1 through F4 and Fm, respectively. Fm will always be turned on since it is directly operated by Rm. Since all the desired information has been stored in a stage of buffer flip-flops, it now becomes possible to destroy the information in the shift register and clear it in preparation for receiving new digits. This is done by allowing one of the inputs of the -H stage to be Rm. Then, when Rm occurs, it produces a -H which inhibits all the regeneration gates in the shift register flip-flops, and consequently clears them.

One thing more must be accomplished before the first wire pulse of the next character may be read into the shift register. A new marker must be created. It also is obtained from Rm through a delay line in the R1 stage.

After the information has been read into the row of buffer flip-flops and the shift register has been cleared and given a marker pulse, two things happen simultaneously; namely, a character is punched on the tape and new information is read into the shift register. The latter operation has been described. It now remains to describe the means by which a character is punched.

Each of the buffer flip-flops, F1 through F4 (or F6), has either been turned on or off according to whether there is a "one" or a "zero" to be punched. Fm is turned on every time. The outputs of each flip-flop are taken from the two output windings of the associated transformer. These windings are connected to double-input gates whose arrangements are that of full-wave rectifiers. The d-c output of each stage is approximately 17 volts which drives a relay. Each relay, if it is energized, allows 110 volts d-c to be applied to a solenoid on the punch. This sets up a "one" or "zero" in the punch. At the same time, the Fm relay energizes the solenoid on the punch that allows the mechanism to go through one punching cycle. The result of this is that the four-binary digits that were originally in the shift register are now punched as one hexadecimal character on a paper tape.

While the punch is going through its cycle, a contact on the mechanism is closed. This contact is used to clear the information from the buffer flip-flops. Since the corresponding relays are no longer energized, they fall out and the whole mechanism is ready for the next cycle of operation.

It was mentioned previously that error checking is done during a gap in the wire pulses. The stage that performs this function is labeled W on Drawing No. 204C. When this stage is turned on, it closes a relay which halts the wire and lights a neon. An AND-gate driving this stage has two inputs. One comes from the gap senser, and so is on only during a gap. The other comes from a large OR-gate which senses stages R1 through R6 and B. If any of these stages is on during the gap, W will be turned on and an error halt will result. By switching arrangements that will be described, the wire is made to stop if an error halt occurs.

The input to the W stage that comes from the gap senser comes by way of F5 acting as a dummy repeater stage. As a result, whenever a gap occurs during four-channel operation, relay L5 is energized and the first character punched after a gap will have a fifth hole to signify that it is the beginning of a block of information.

C. Timing and Its Relation to the Punch

In the operation of punching a tape with the Flexowriter punch that is used in conjunction with the Outscriber, the timing of the various operations is very important for proper punching. Furthermore, unlike the electronic circuitry, there is no automatic checking mechanism for the punching operation. Only by careful adjustment of the timing can reliable punching be obtained.

The timing of the whole cycle of operation is shown in Figure 7. Operation up to the time when the F flip-flops are turned on has already been described. When these flip-flops go on, they energize their corresponding relays. It will be seen that the relay contacts close nine milliseconds after their coils are energized. Actually, this figure represents an average, the times corresponding to individual relays ranging from 6 to 12 milliseconds.

The main shaft of the punch rotates continuously. The punching mechanism, however, operates only when a spring clutch is released. To do this, an iron armature which engages a cam on the clutch cylinder is attracted by a solenoid energized through the contacts of relay Lm. When this solenoid is energized, the punch mechanism performs one cycle of operation at the end of which, if the armature has returned to its rest position, the mechanism comes to rest. The repetition rate should never exceed 12.5 cycles per second. In practice a repetition rate of about 10 characters per second is used.

Before the punch mechanism is set into rotation, information from the relays is used to set up so-called punch fingers. These fingers have two stable positions: latched, corresponding to no hole, and unlatched, corresponding to a hole in the tape. The latches are released by energizing the information solenoids. After the punch fingers are set, the clutch mechanism may be released. As soon as the clutch grips, the main shaft begins rotating. A fraction of a cycle later, lockout spears engage the previously set fingers. These spears force the fingers to remain in the state in which they have been set. Not until

shortly before the end of the cycle, when the lockout spears are released, are the fingers reset. It is while the fingers are set in position that the punching operation takes place. There is also a contact that operates simultaneously with the spears, closing when they are set and opening when they are reset.

Since all relays are energized simultaneously, their contacts close at a time that differs only insofar as there are differences in individual mechanical construction. Four milliseconds after relays L1 through L4 close, their corresponding fingers are set, while seven milliseconds after Lm closes, the clutch armature is disengaged. All that is necessary is that the fingers be set before the clutch armature becomes disengaged. However, because of the large variation between individual pull-in times of the relays, it is desirable to select relay Lm such that its pull-in time is the longest of those of the relays used.

For energizing the finger solenoids, a special voltage waveform must be used. In order reliably to pull-in the armatures, 110 volts d-c is required. However, if regulated 110 volts d-c is used, the coils will heat unnecessarily. Under normal loading, after about 50 milliseconds this supply voltage drops to 55 volts, whereas four milliseconds after it is loaded and when the fingers are still being pulled in, the voltage has only dropped to 87 volts in the worst case. The 55 volts steady state is sufficiently low to prevent overheating in the coils with the duty cycle that is used.

Once the lockout spears are "in", it becomes possible to clear all circuits since the information is held in the punch fingers. This is done by using the contact that closes when the lockout spears come in to clear the row of buffer flip-flops. By putting -10 volts on the regeneration gates in stages F1 through Fm, those flip-flops are all turned off, whereas when the clearing contact is open, a 1K pull-up resistor to +4 volts allows information to regenerate through the gates.

When the buffer flip-flops are cleared, their corresponding relays are deenergized and they begin to open. In order to decrease this "fall-out" time, pieces of .002-inch brass are sweated to the relay armatures. Without this precaution the relay contacts will not always be open in time for the next punching cycle.

Not only must the information relays be open before the next cycle, but the relay which drives the clutch solenoid must open soon enough for the latching armature to latch the rotating shaft when the punch shaft returns to its rest position. If this does not happen, the punch will run through one "free" cycle. This will result in an erratic punching rate and the punching of zeros instead of proper information since the punch would operate before the information fingers could be set.

If at any time the punch should miss one cycle because of some electrical or mechanical fault, it may stop indefinitely until appropriate switches are operated. This is caused by the poor regulation of the 110-volt power supply which drives the punch solenoids. When the punch fails for one cycle, the contact on the lockout spears is not closed. As a result, the row of F flip-flops remains on and each corresponding relay stays closed. This maintains the punch solenoid load on the power supply. However, because of the poor voltage-time regulation, by the time the next punch cycle begins, the power supply voltage has dropped so low as to be unable to disengage the clutch armature, and the punch remains at rest.

D. Power and Signal Switching

In the several cases described, it has been assumed that such voltages appeared at various points as to cause the operation described. Actually, the condition of the various switches on the switching chassis determine many of the connections in the Outscriber. The functions of the individual switches will be given here, rather than the complicated wiring of the switching chassis. Tracing of the actual wiring as shown in Drawing No. 204C will be left to the reader.

On the switching chassis is located the reset button. When operated, it puts the high-speed circuitry in the state it is in before wire pulses occur. To do this, the binary counter must be returned to the zero state, all information must be destroyed in the shift register and in the buffer flip-flops, and a marker must be put into R1.

To clear the binary counter, two AND-gates in the B stage must be turned off. This is done by applying -10 volts to the inputs that are normally at +4 volts. This same voltage is used for clearing the F flip-flops. To destroy all the information in the shift register -H pulses are generated when the reset button is pressed. This is done by applying a

PROCEDURE FOR OPERATING THE OUTSCRIBER

A standard procedure for using the Outscriber has been devised, which is best described in reference B1, Haueter, R., The Outscriber, TM-12.3-10, March 26, 1953.

VI. REFERENCES

A. Drawings

1. Drawing Nos. 2040, Outscriber Functional Diagram
2. Drawing No. 209, Outscriber Package Layout
3. Drawing No. G-3C STATAC Package Configuration
4. Drawing No. 211 (included as Figure 3)

Outscriber Amplifier Schematic

B. Reports and Technical Memoranda

1. Haueter, R.J. The Outscriber, TM-12.3-10, March 26, 1953.
2. Wait, R. Data Forms of Packages for Use in STATAC, TM-12.3-6, June 25, 1951.
3. Haueter, R., Auxiliary Equipment to SEAC Input-Output, Review of Input-Output Equipment in Computing Systems, Joint AIEE-IRE-ACM Conference, pp. 39-44, March 1953.

C. Figures

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2. Cable Connections of Outscriber
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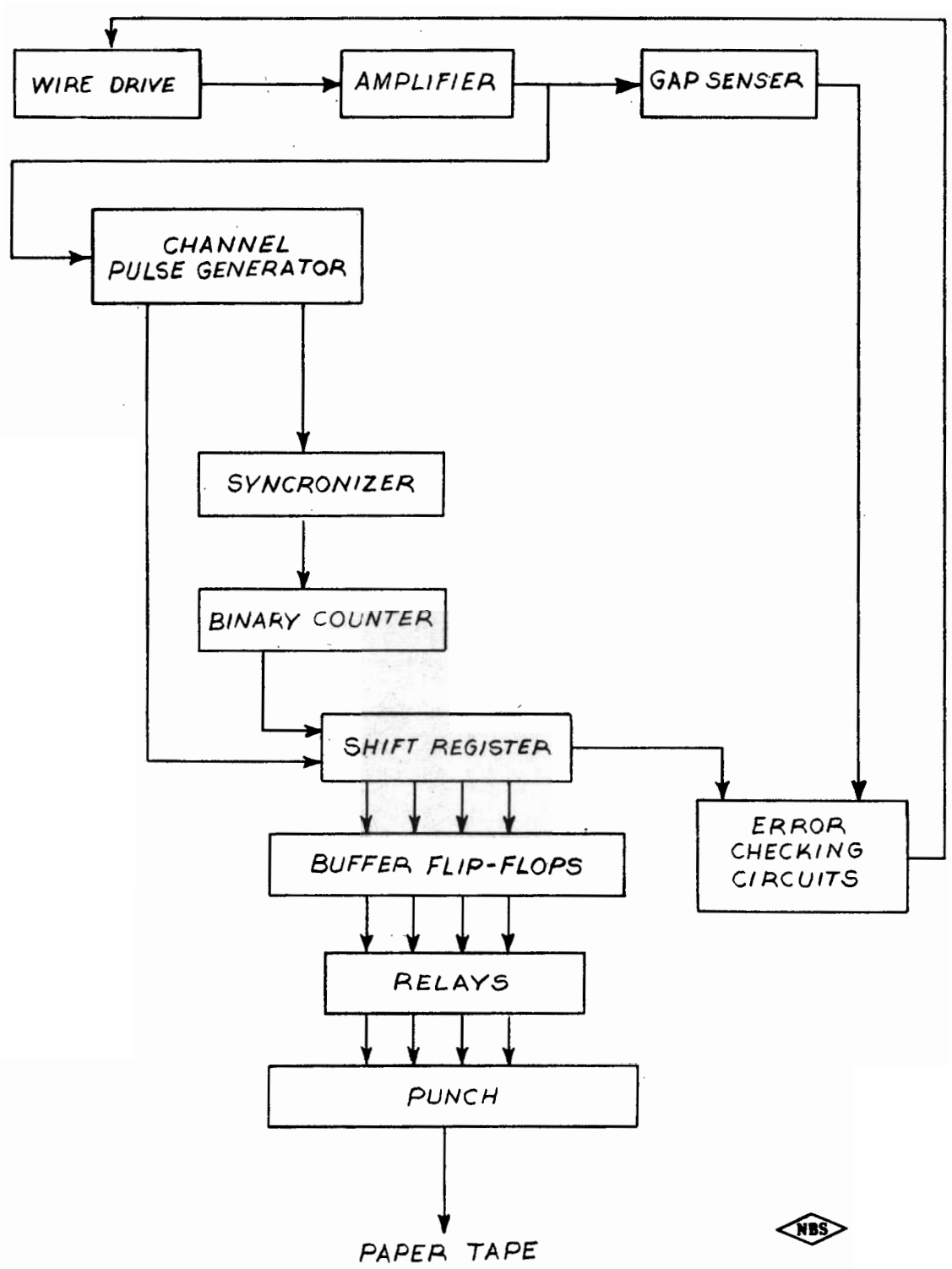

Figure 1. Over-all Block Diagram of the Outscriber

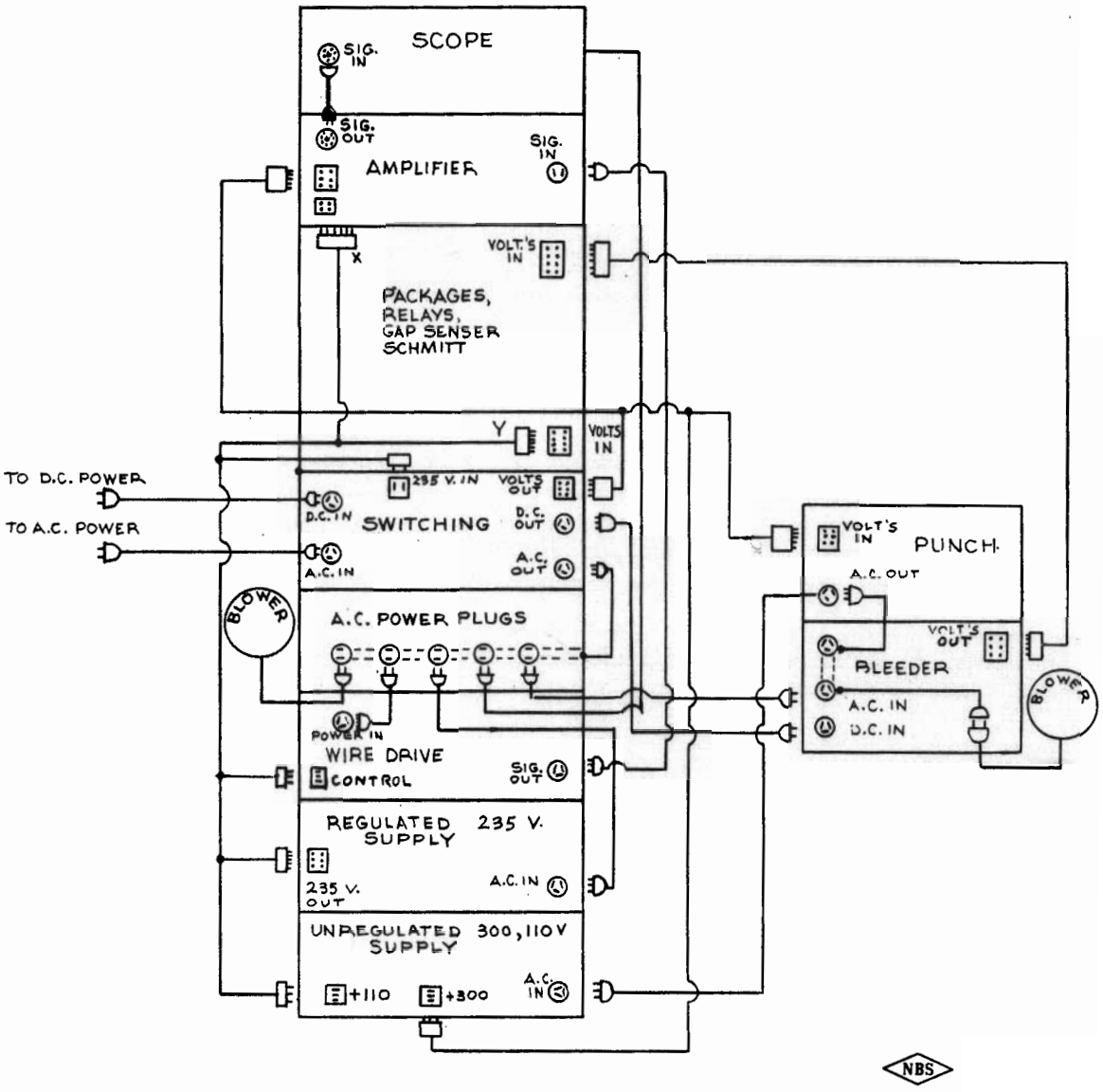

Figure 2. Cable Connections of Outscriber

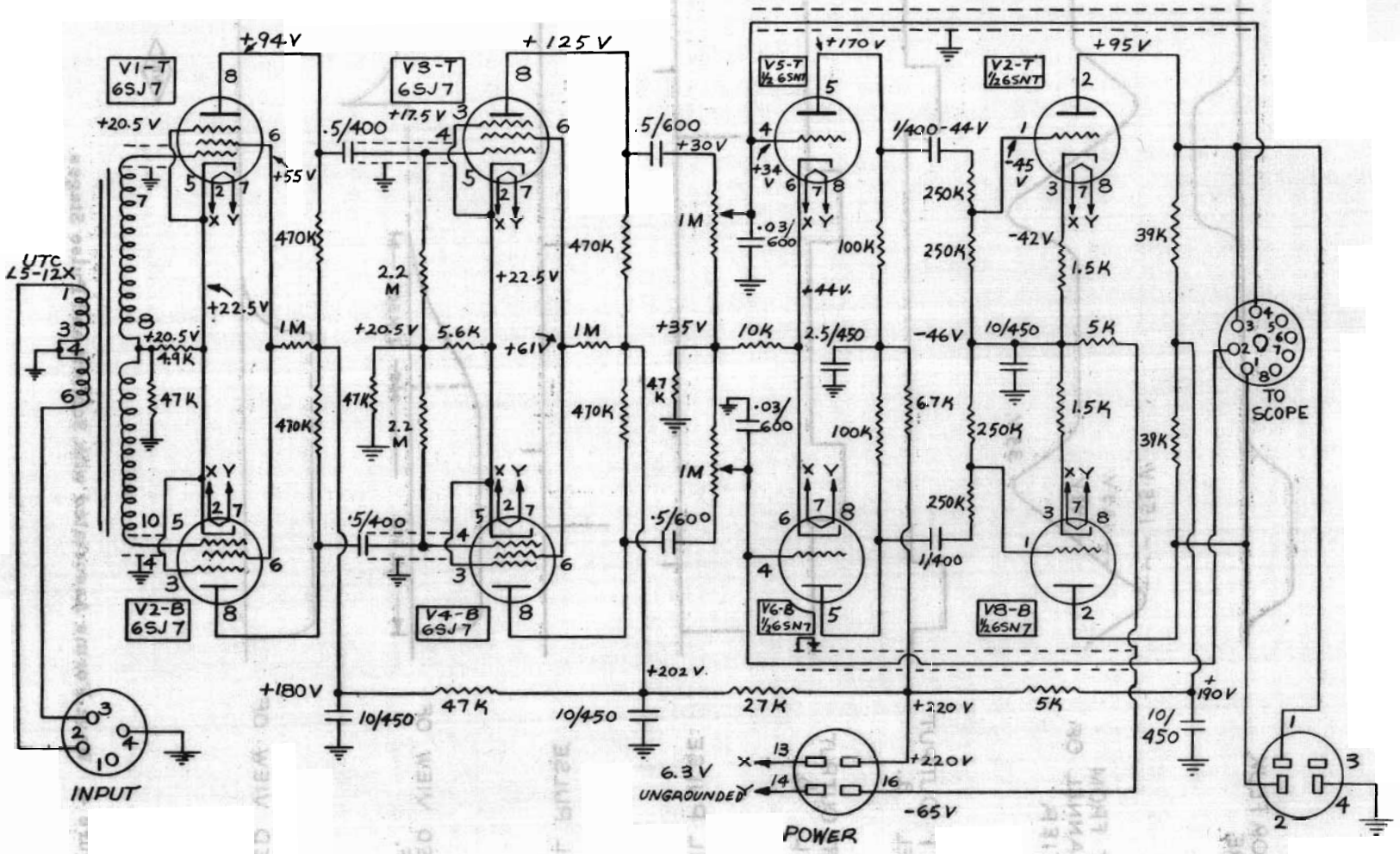

Figure 3. Outscriber Amplifier Schematic with Voltage Points

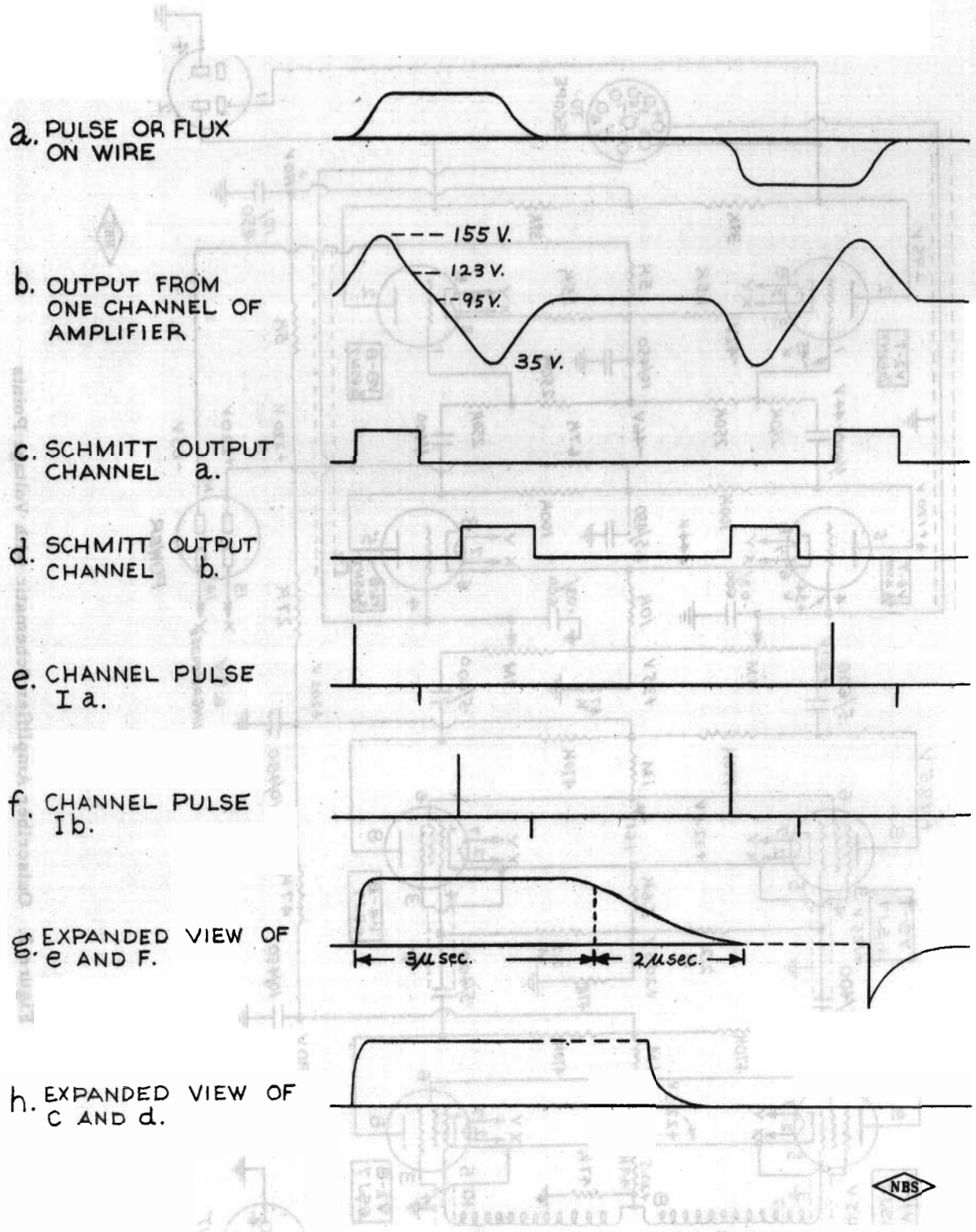

Figure 4. Wave Forms Associated with Schmitt and Pulse Stages

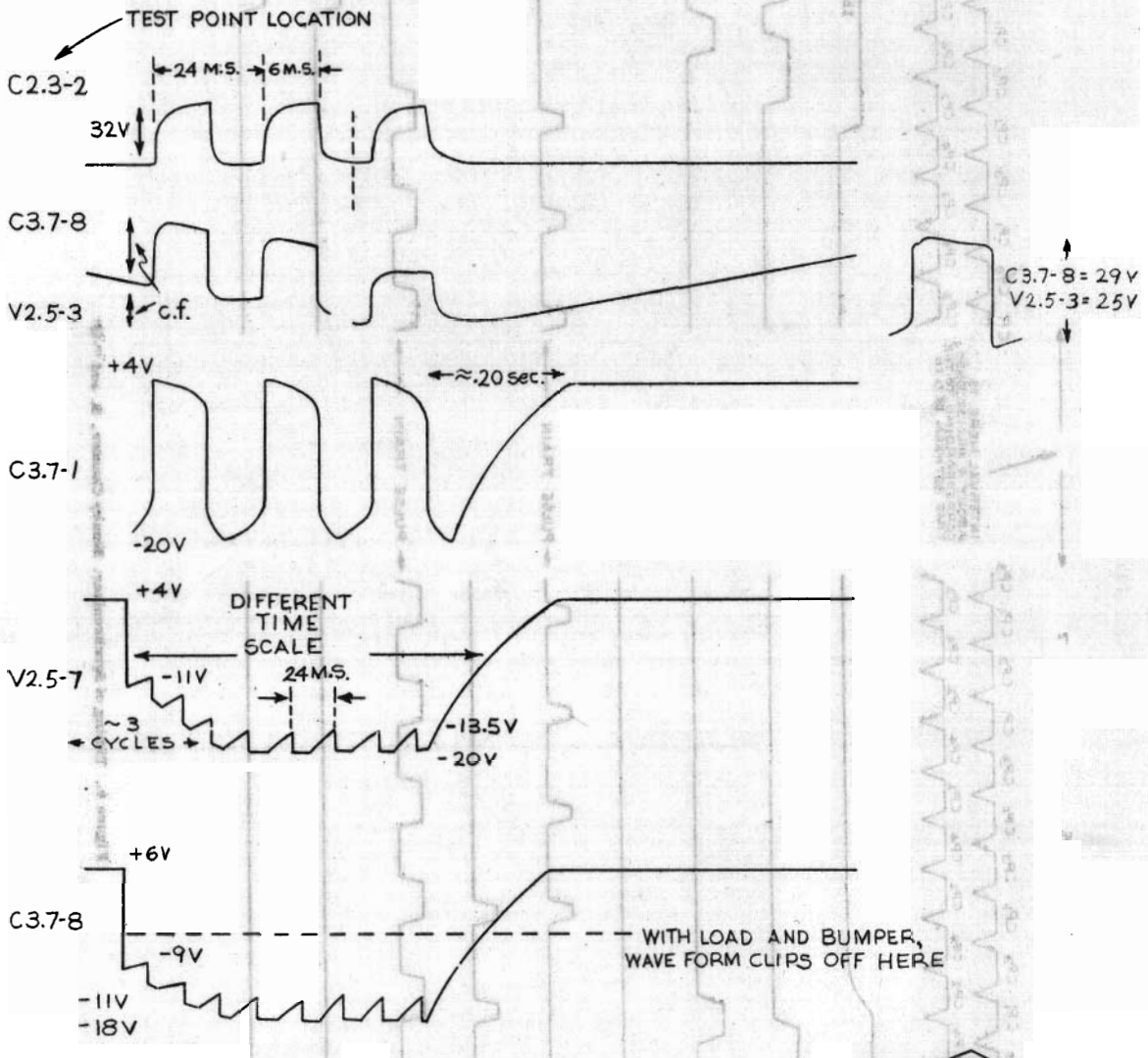

Figure 5. Gap Sense Circuit Wave Forms

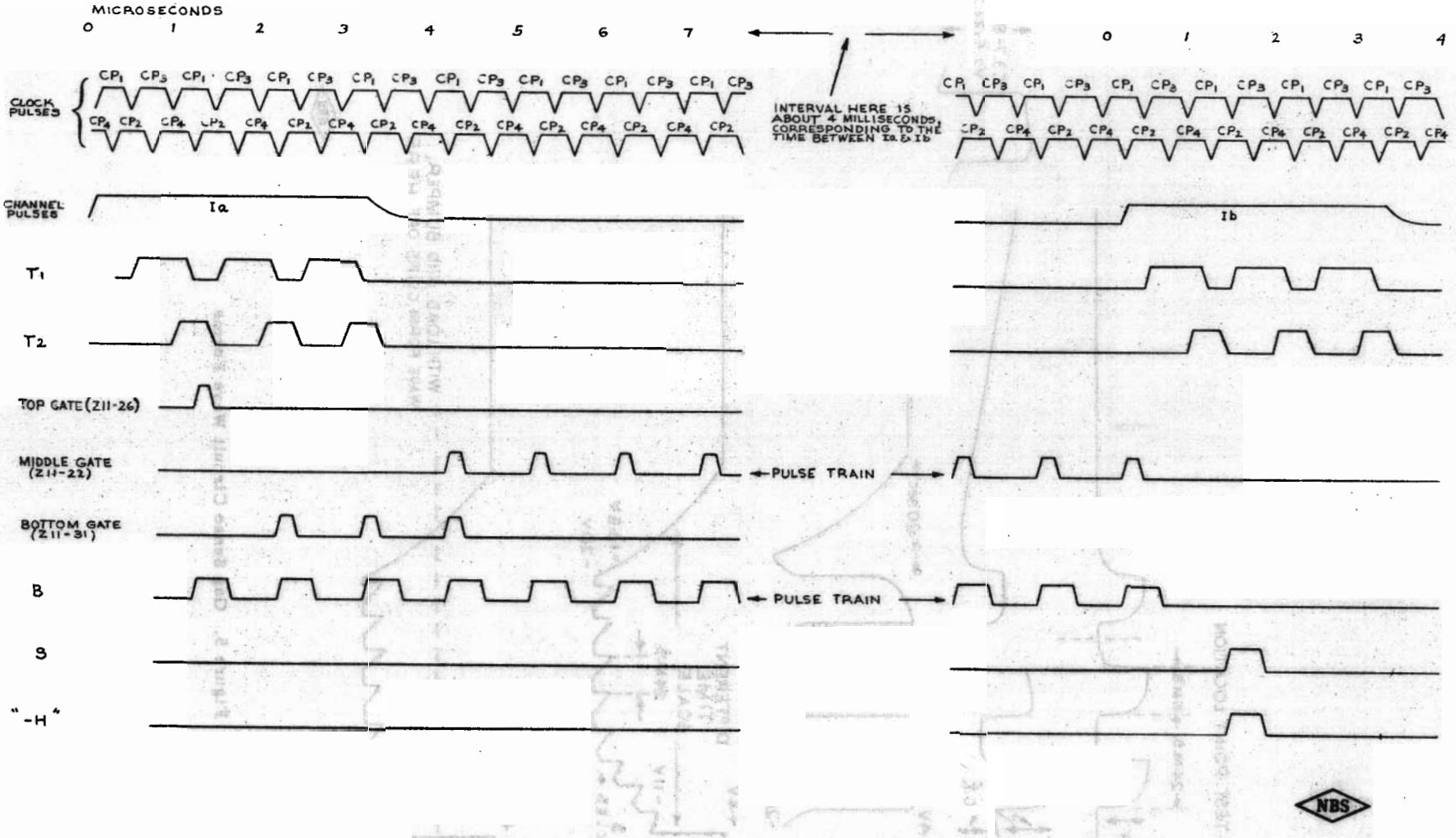

Figure 6. Timing of Synchronizer, Binary Counter, S, and "-H"

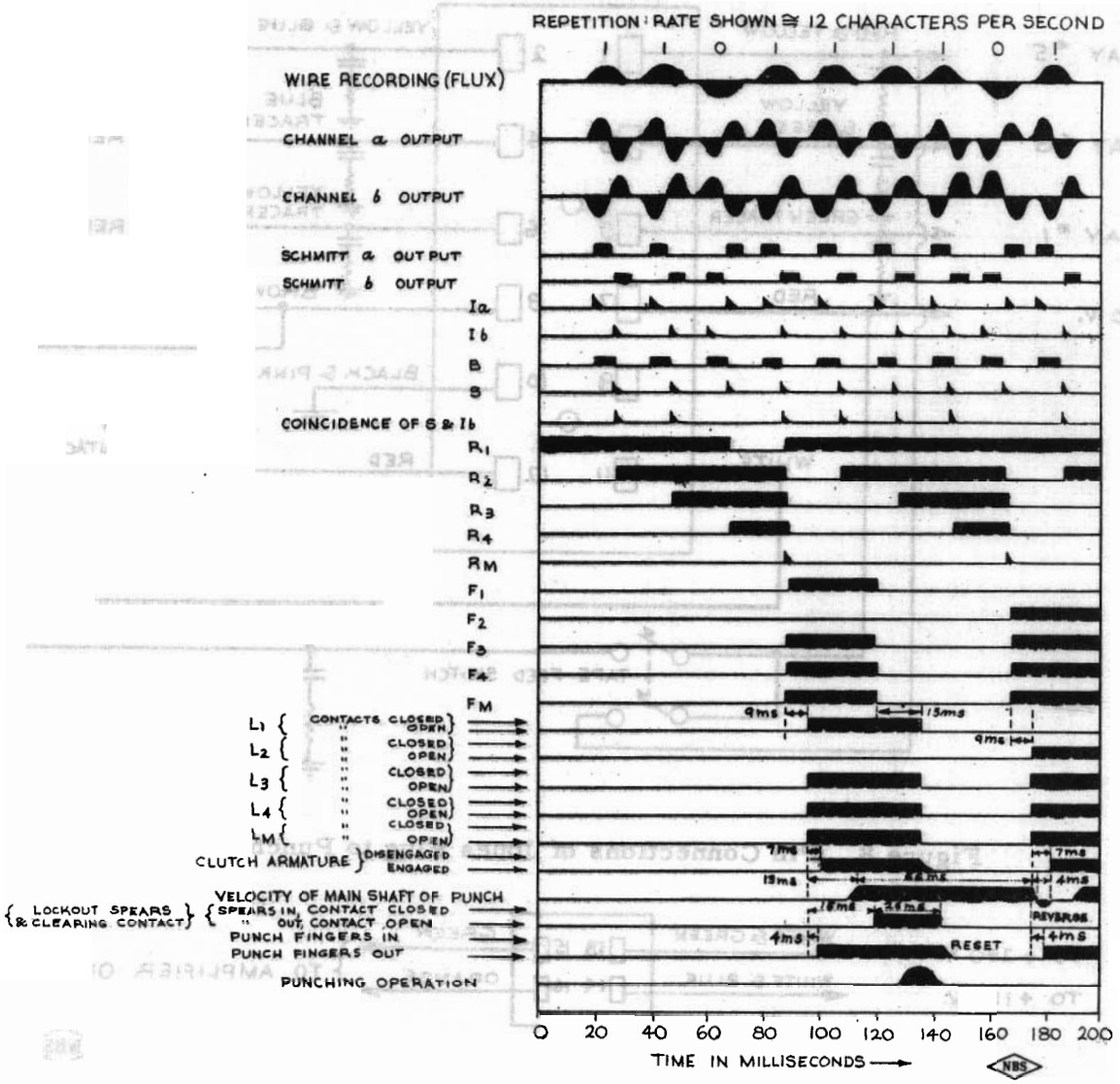

Figure 7. Timing Diagram of the Outscriber

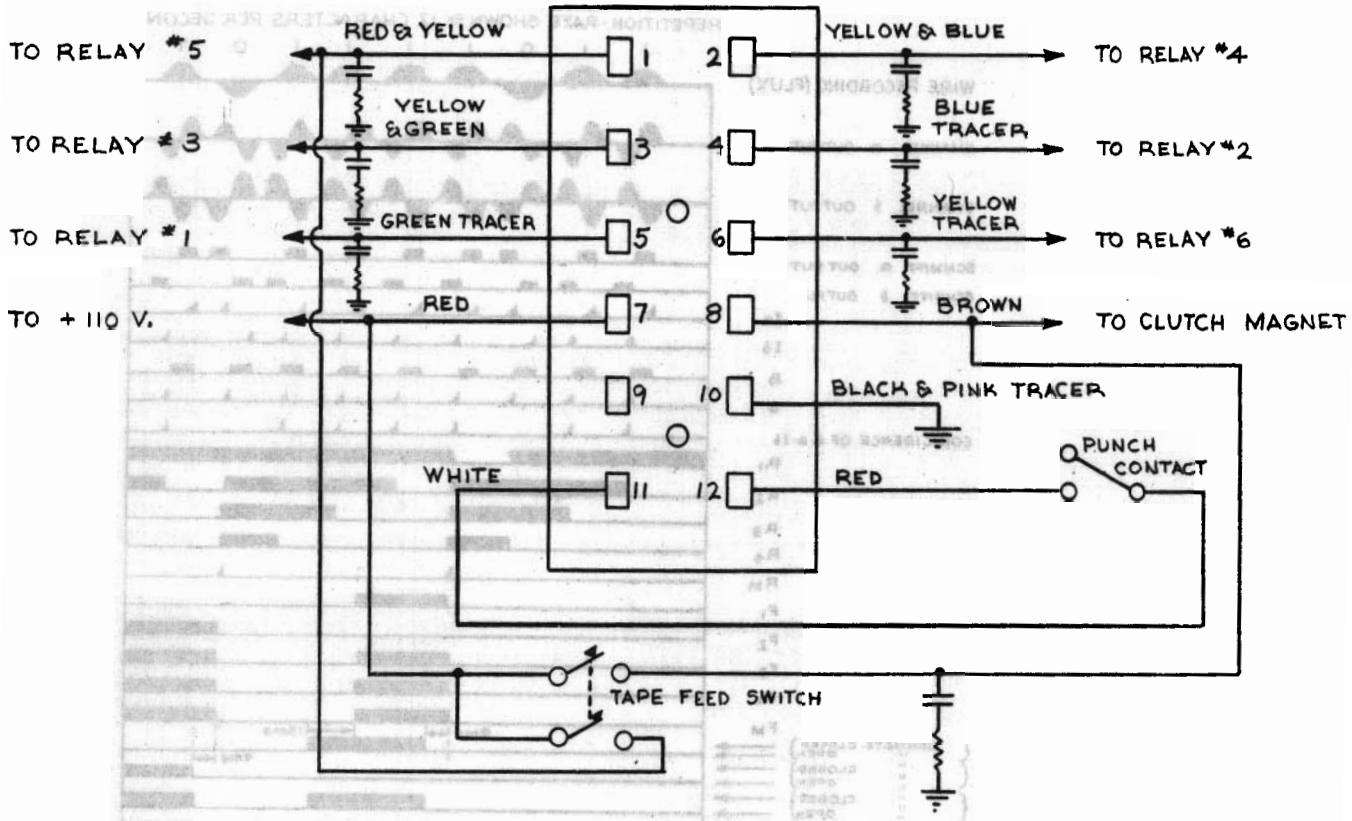

Figure 8. Pin Connections of Jones Plug to Punch

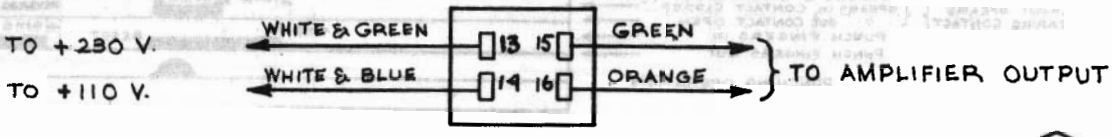

Figure 9. Pin Layout of Four Pin Jones Plug on Package Chassis

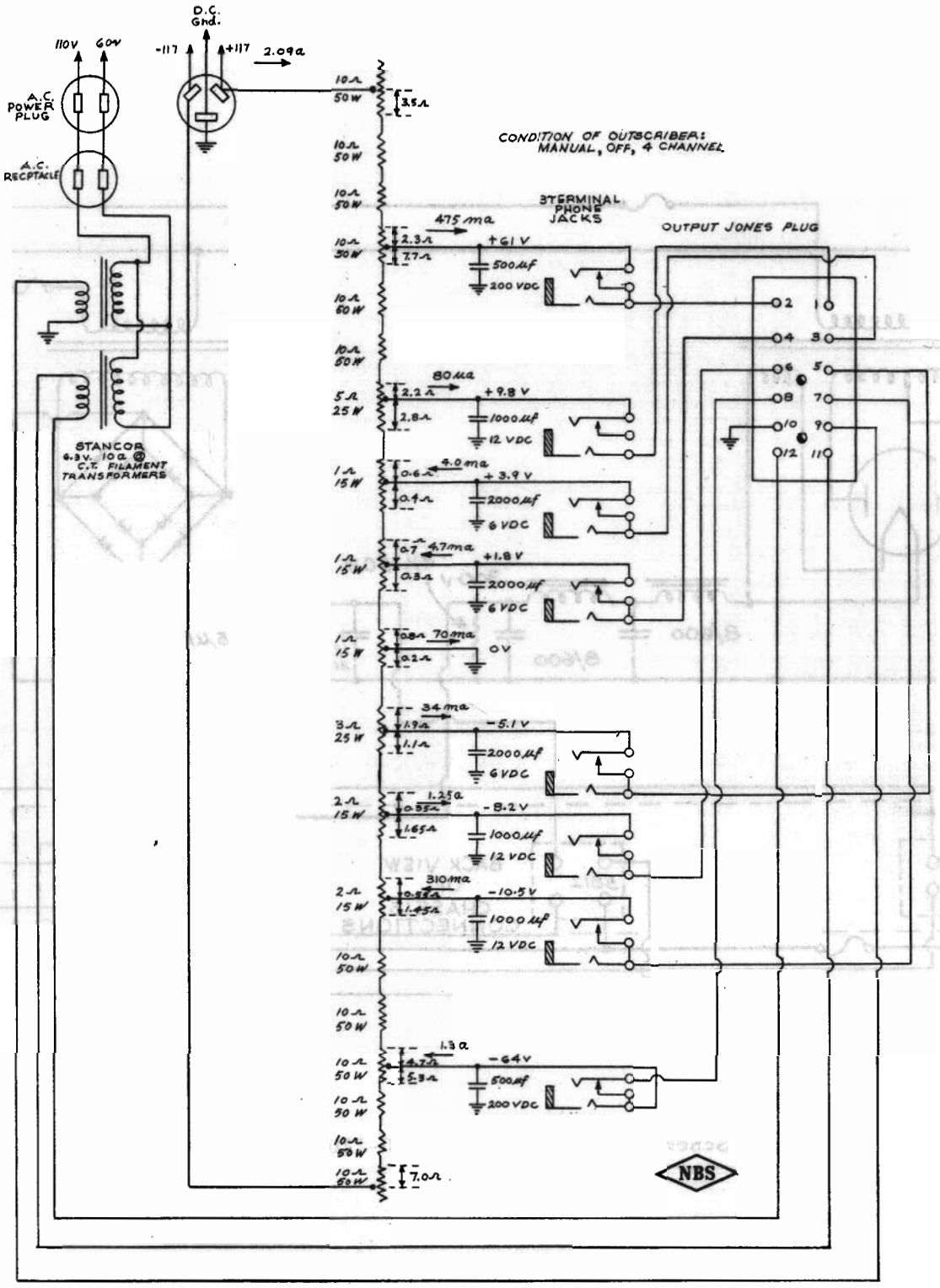

Figure 10. Schematic of Power Bleeder Supply of Outscriber Showing Static Current Drain and Voltage Points

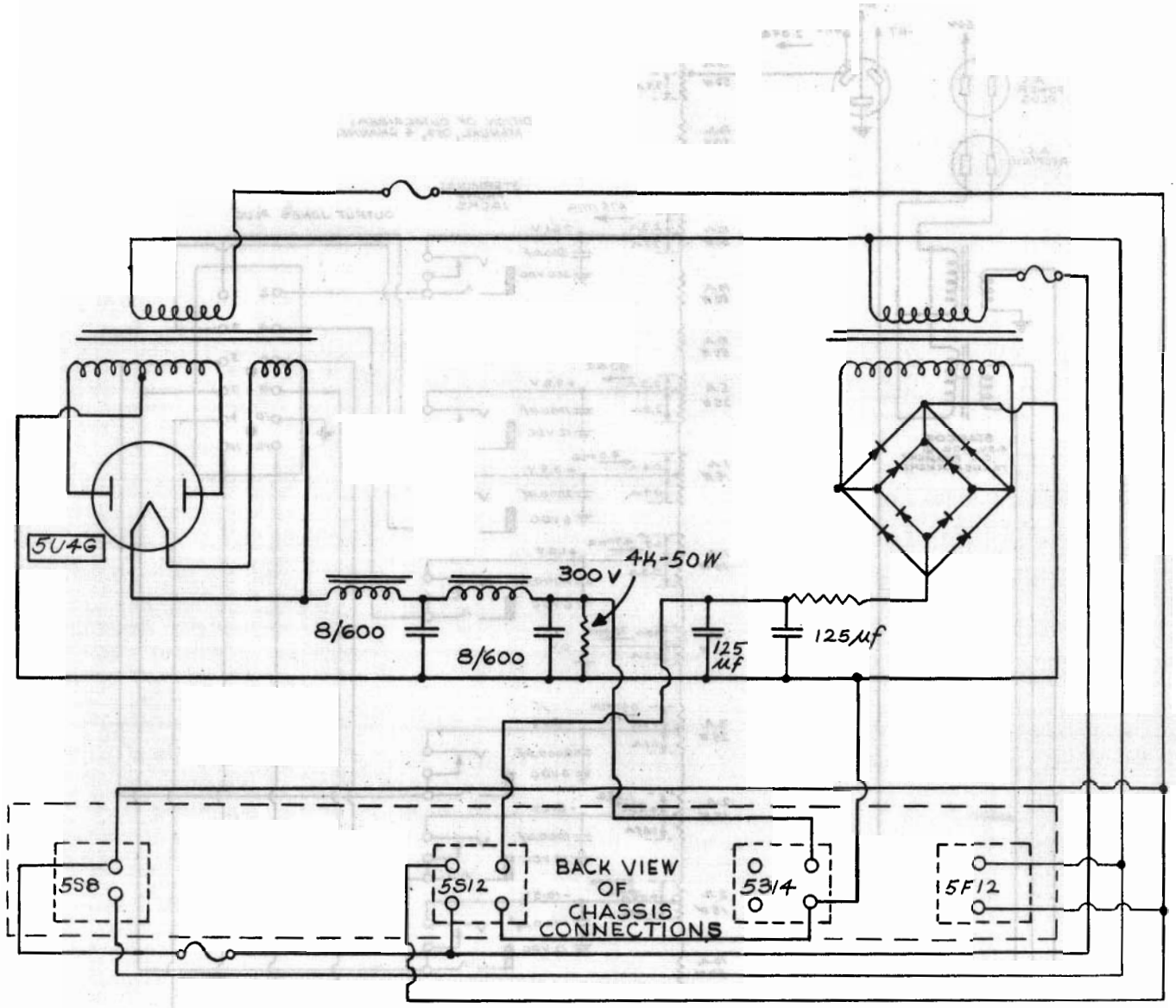

Figure 11. Schematic of Unregulated 300-120 Volt Power Supply

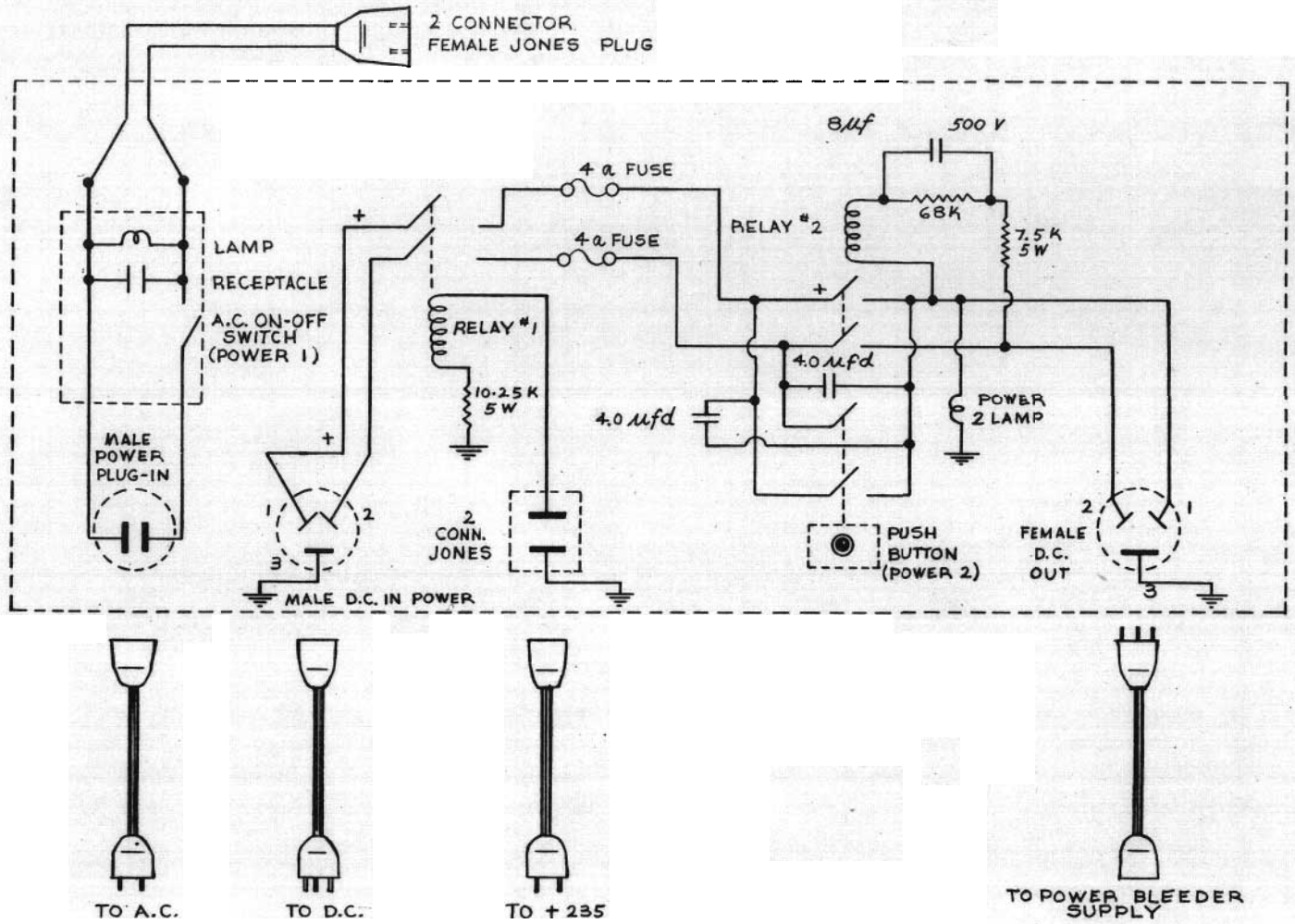

Figure 12. Power Switching Chassis

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